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H HOLMES: Capturing the Yield/Optimized Design Space Boundaries of Analog and RF Integrated Circuits Bart De Smedt and Georges Gielen ESATMICAS, Kasteelpark Arenberg 10, B3001 Leuven, Belgium (Bart.DeSmedt, Georges.Gielen)@esat.kuleuven.ac.be Abstract A novel methodology is presented to structured yield optimize {?d x, ? , Y x, ? } (1)aware synthesis. The tradeoff between yield andthe unspeci?ed pe...

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